Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_

G:\logo and QP Template\logo 3 Feb 2018 final.tif

**End Semester Examination – Nov/Dec – 2018**

|  |  |  |  |
| --- | --- | --- | --- |
|  |  |  |  |
| **Code :** | **17EC3036** | **Duration :** | **3hrs** |
| **Sub. Name :** | **LOW POWER VLSI DESIGN** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | A 128 bit off-chip bus operating at 3.5 V and 1GHz clock rate is driving a capacitance of 60 pF/ bit. Each bit is estimated to have a toggling probability of 0.5 at each clock cycle. Analyse the power dissipation in operating the bus? | CO1 | 5 |
| b. | Discuss the variation of short circuit current of a CMOS inverter for input signal slope and output load capacitance. | CO1 | 15 |
| (OR) | | | | |
| 2. | a. | The chip size of a CPU is 30 mm x 60 mm with clock frequency of 600 MHz operating at 2.5 V. The length of the clock routing is estimated to be thrice the circumference of the chip. Assume that the clock frequency is routed on a metal layer with the width of 1.8µm and the parasitic capacitance of the metal layer is 1.5 Ff/µm2. Calculate the power dissipation of the clock signal? | CO1 | 5 |
| b. | Justify the need for Low Power VLSI chips. | CO1 | 5 |
| c. | Summarise the components of leakage currents in CMOS circuits. | CO1 | 10 |
|  |  |  |  |  |
| 3. | a. | Derive an expression which relates static probability and frequency. | CO3 | 5 |
| b. | Evaluate the transition density and static probability of y= ab + c given P (a) = 0.3, P (b) = 0.4, P(c) = 0.2, D(a) = 2, D(b) =3,  D(c) = 4. | CO3 | 15 |
| (OR) | | | | |
| 4. | a. | Derive the expressions for the power and delay of an inverter chain using transistor sizing. | CO2 | 12 |
| b. | Apply the equivalent pin ordering concept to the two input NAND gate. | CO2 | 8 |
|  |  |  |  |  |
| 5. | a. | Construct the 4X4 array multiplier without glitches. | CO4 | 10 |
| b. | Select any one technique to reduce power in magnitude comparator. | CO4 | 10 |
| (OR) | | | | |
| 6. | a. | Apply the power and performance management techniques to reduce power in architecture level. | CO4 | 10 |
| b. | Choose one technique to reduce power in digital filters. | CO4 | 10 |
|  |  |  |  |  |
| 7 | a. | Explain the operation of 6T SRAM circuit with diagram. | CO5 | 5 |
| b. | Describe the methods to reduce power in write drivers and sense amplifier in SRAM architecture with neat diagrams. | CO5 | 15 |
| (OR) | | | | |
| 8. |  | Explain the banked SRAM concepts and also the techniques to reduce the voltage swings on bit lines in SRAM design. | CO5 | 20 |
|  | | **Compulsory**: |  |  |
| 9. |  | Analyse the various performance measures for latches and flip-flops. | CO6 | 20 |